

### **Abstract of the Disclosure**

A method for forming gate segments in an integrated circuit. The method begins by forming a shallow trench isolation region outwardly from a layer of semiconductor material to isolate a plurality of active regions of the integrated circuit. After the isolation region is formed, at least one gate segment is formed in each active region by depositing, planarizing and selectively etching a conductive material. Source/drain regions are also formed in the active region. The active regions are selectively interconnected with edge-defined conductors that pass outwardly from the gate segments and the shallow trench isolation region to form the integrated circuit.

10

"Express Mail" mailing label number: EV298566393US

Date of Deposit: September 19, 2003

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.